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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/801,093	HANAOKA ET AL
	Examiner	Art Unit
	Ben P. Sandvik	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 12, 14, 16, 17, and 19 rejected under 35 U.S.C. 102(b) as being anticipated by Elenius et al (U.S. Patent #6287893), hereafter known as Elenius.

i. With respect to **claim 12**, Elenius teaches a semiconductor chip having an integrated circuit (Fig. 2, 12 and Col 6 Ln 5-7) and a pad electrically connected to the integrated circuit (Fig. 2, 18), a wiring layer electrically connected to the pad and having a concave portion, the concave portion being formed in such a way that an angle between as osculating plane at any point of a surface of the concave portion and a top surface of the wiring layer, with the angle defined outside the concave portion, is 90° (Fig. 2, 30), an external terminal joined to the concave portion of the wiring layer (Fig. 2, 28), a resin layer provided on the wiring layer, the resin layer having a through hole, the through hole and the concave portion overlapping each other (Fig. 2, 33 and Col 7 Ln 53).

ii. With respect to **claim 14**, the concave portion has a width that decreases with a depth of the concave portion (Fig. 2, 30).

iii. With respect to **claim 16**, Elenius teaches that the external terminal contacts the through hole in the resin layer (Fig. 2, 28).

iv. With respect to **claim 17**, Elenius teaches a stress relief layer formed above the semiconductor chip wherein the wiring layer is formed above the stress relief layer (Fig. 2, 24).

v. With respect to **claim 19**, Elenius teaches a circuit board including the semiconductor device according to claim 12 (Col 9 Ln 57).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 18, 20, 21, 23, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius, in view of Kuwabara et al (U.S. PG Pub #20020008320).

vi. With respect to **claim 18**, Elenius teaches all of the limitations of claim 12, but does not teach that the resin layer is formed of a solder resist. Kuwabara teaches a resin layer formed of a solder resist (Paragraph 108). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the package of Elenius with a solder resist layer as taught by Kuwabara in order to protect the wiring layer.

vii. With respect to **claim 20**, Elenius teaches all of the limitations of claim 12, but does not teach an electronic instrument including the semiconductor device according to claim 12. Kuwabara teaches an electronic instrument (Fig. 21, 1200). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the semiconductor package of Elenius in an electronic device as taught by Kuwabara in order to make a functioning and usable device.

viii. With respect to **claims 21, 23, and 25-27**, Elenius teaches a semiconductor chip having an integrated circuit (Fig. 2, 12 and Col 6 Ln 5-7) and a pad electrically connected to the integrated circuit (Fig. 2, 18),

a wiring layer electrically connected to the pad and having a concave portion, the concave portion being formed in such a way that an angle between as osculating plane at any point of a surface of the concave portion and a top surface of the wiring layer, with the angle defined outside the concave portion, is 90° (Fig. 2, 30),

an external terminal joined to the concave portion of the wiring layer (Fig. 2, 28), a resin layer provided on the wiring layer, the resin layer having a through hole, the through hole and the concave portion overlapping each other (Fig. 2, 33 and Col 7 Ln 53),

a concave portion has a width that decreases with a depth of the concave portion (Fig. 2, 30),

an external terminal contacts the through hole in the resin layer (Fig. 2, 28),

and a stress relief layer formed above the semiconductor chip wherein the wiring layer is formed above the stress relief layer (Fig. 2, 24).

Elenius does not teach that there is a plurality of semiconductor packages disposed on a single wafer, or a resin layer formed of a solder resist. Kuwabara teaches a plurality of semiconductor packages disposed on single wafer (Fig. 1), and a solder resist layer (Paragraph 108). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a plurality of semiconductor packages as taught by Elenius on a single wafer as taught by Kuwabara in order to lower manufacturing costs, and to provide a solder resist layer on the package of Elenius as taught by Kuwabara in order to protect the wiring layer.

3. Claims 1, 2, 5, 7, 8, 9, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius, in view of Iwasaki (U.S. PG Pub #20020167013).

ix. With respect to **claims 1, 2, 5, 7, 8, 9, and 10**, Elenius teaches the formation of a wiring layer (Fig. 2, 30) on a semiconductor substrate having an integrated circuit (Fig. 2, 12 and Col 6 Ln 5-7) and a pad electrically connected to the integrated circuit (Fig. 2, 18), the wiring layer being electrically connected to the pad, the formation of a resin layer covering the wiring layer (Fig. 2, 33 and Col 7 Ln 53), forming a second

concave portion in the wiring layer in such a way that an angle between an osculating plane at any point of a surface of the second concave portion and a top surface of the wiring layer; with the angle being defined outside the second concave portion is 90° or more (Fig. 2, 30), providing an external terminal in the second concave portion of the wiring layer (Fig. 2, 28), and providing the second concave portion with a width that decreases with a depth of the second concave portion (Fig. 2, 30).

x. Elenius does not teach the formation of a first concave portion at an area of the resin layer, the area overlapping the wiring layer, by a first process, the formation of a through hole in the resin layer by removing a bottom of the first concave portion by a second process, the second process differing from the first process, that the first concave portion is formed in such a way that an angle between an osculating plane at any point of a surface of the first concave portion and a top surface of the wiring layer; with the angle being defined outside the first concave portion is 90° or more, that the second process comprises dry etching, providing the first concave portion with a curved outline at a cross section taken along a plane perpendicular to a top surface of the resin layer, providing the second concave portion with a curved outline at a cross section taken along a plane perpendicular to the top surface of the wiring layer, or providing the first concave portion with a width that decreases with a depth of the first concave portion.

xi. Iwasaki teaches the formation of a first concave portion (Fig. 10b, 55), the formation of a through hole by a second process, the second process differing from the first process (Fig. 10c, 53 and Paragraph 128), that the first concave portion is formed in such a way that an angle between an osculating plane at any point of a surface of the first concave portion and a top surface of the wiring layer; with the angle being defined outside the first concave portion is 90° or more (Fig. 10b, 55), that the second process comprises dry etching (Paragraph 128), providing the first concave portion with a curved outline at a cross section taken along a plane perpendicular to a top surface of the resin layer (Fig. 10b, 55), providing the second concave portion with a curved outline at a cross section taken along a plane perpendicular to the top surface of the wiring layer (Fig. 10c, 53), or providing the first concave portion with a width that decreases with a depth of the first concave portion (Fig. 10b, 55).

xii. It would have been obvious to one of ordinary skill in the art at the time the invention was made to begin the process of etching the resin layer of Elenius by forming a first concave portion as taught by Iwasaki in order to concentrate the etching process on a specific area, and to form a through hole in the resin of Elenius by a second process as taught by Iwasaki in order to facilitate a connection to the wiring layer, to form the first concave portion in such a way that an angle between an osculating plane at any point of a surface of the first concave portion and a top

surface of the wiring layer; with the angle being defined outside the first concave portion is 90° or more in order to focus the etching process on a specific area, to have the second process comprise dry etching as taught by Iwasaki in order to easily fabricate the through hole, to provide a first and second concave portions with a curved outline as taught by Iwasaki in order to create a smooth interface between the external terminal and wiring layer, and to provide the first concave portion with a width that decreases with a depth as taught by Iwasaki in order to focus the etching process on a specific area.

xiii. With respect to **claim 13**, Elenius teaches all of the limitation of claim 12, but does not teach a concave portion having a curved outline at a cross section taken along a plane perpendicular to the top surface of the wiring layer. Iwasaki teaches concave portion having a curved outline at a cross section taken along a plane perpendicular to the top surface of the wiring layer (Fig. 10c, 53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the concave portion with a curved outline as taught by Iwasaki in order create a smooth interface for a connection between the wiring layer and the external electrode.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius and Iwasaki, in view of Imai (U.S. Patent #5266501).

xiv. With respect to **claim 3**, Elenius and Iwasaki teach all of the limitations of claim 1, but do not teach that the resin layer is formed of a thermosetting resin precursor and, prior to step (d), the thermosetting resin precursor is heated. Imai teaches a process where a resin layer is formed of a thermosetting resin and heated (Col 3 Ln 36-43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a resin layer as taught by Elenius and Iwasaki with a thermosetting resin in order to protect the surface of the package.

5. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius and Iwasaki, in view of Schiltz et al (U.S. Patent #6387808).

xv. With respect to **claim 4**, Elenius and Iwasaki teach all of the limitations of claim 1, and furthermore Iwasaki teaches that the first process includes irradiation. Elenius and Iwasaki do not teach the formation of the resin layer of a resin precursor that is sensitive to radiation. Schiltz teaches a resin layer that is sensitive to radiation and is developed with irradiation (Fig. 2a, 20 and Col 2 Ln 45-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the resin layer of Elenius and Iwasaki out of a resin precursor that is sensitive to radiation and is developed by radiation in order to protect the surface of the package.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius and Iwasaki, in view of Kuwabara.

xvi. With respect to **claim 6**, Elenius and Iwasaki teach all of the limitations of claim 1, but do not teach a resin layer of a solder resist. Kuwabara teaches a resin layer of a solder resist (Paragraph 108). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the package of Elenius and Iwasaki with a solder resist layer as taught by Kuwabara in order to protect the wiring layer.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius and Iwasaki, in view of Hwang et al (U.S. Patent #6455408).

xvii. With respect to **claim 11**, Elenius and Iwasaki teach all of the limitations of claim 1, but do not teach forming the second concave portion in such a way that an opening thereof is entirely disposed inside the through hole. Hwang teaches forming a concave portion in such a way that an opening thereof is entirely disposed inside the through hole (Fig. 17, 78). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the second concave portion of Elenius and Iwasaki to have an opening that is entirely disposed inside the through hole as taught by Hwang in order to make a better connection between the wiring layer and external terminal.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius in view of Hwang.

xviii. With respect to **claim 15**, Elenius teaches all of the limitations of claim 12, but do not teach forming the concave portion in such a way that an opening thereof is entirely disposed inside the through hole. Hwang teaches forming a concave portion in such a way that an opening thereof is entirely disposed inside the through hole (Fig. 17, 78). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the concave portion of Elenius to have an opening that is entirely disposed inside the through hole as taught by Hwang in order to make a better connection between the wiring layer and external terminal.

9. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius and Kuwabara, in view of Iwasaki.

xix. With respect to **claim 22**, Elenius and Kuwabara teach all of the limitation of claim 21, but do not teach concaves portion having a curved outline at a cross section taken along a plane perpendicular to the top surface of the wiring layer. Iwasaki teaches concave portion having a curved outline at a cross section taken along a plane perpendicular to the top surface of the wiring layer (Fig. 10c, 53). It would have been obvious

to one of ordinary skill in the art at the time the invention was made to make the concave portions with a curved outline as taught by Iwasaki in order create a smooth interface for a connection between the wiring layers and the external electrodes.

10. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Elenius and Kuwabara, in view of Hwang.

xx. With respect to **claim 24**, Elenius and Kuwabara teach all of the limitations of claim 21, but do not teach forming the concave portions in such a way that an opening thereof is entirely disposed inside the through hole. Hwang teaches forming a concave portion in such a way that an opening thereof is entirely disposed inside the through hole (Fig. 17, 78). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the concave portions of Elenius and Kuwabara to have an opening that is entirely disposed inside the through hole as taught by Hwang in order to make a better connection between the wiring layer and external terminal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bps

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